CLAIMS

What is claimed is:

1. A write select circuit comprising:

a pulse stretcher stretching clock pulses;

a READ/WRITE decode selectively passing stretched said clock pulses responsive to a write select signal; and

a write driver receiving passed said stretched clock pulses and driving said write select pulses responsive to received said stretched clock pulses.

2. A write select circuit as in claim 1, wherein said write select circuit is a CMOS write select circuit and said pulse stretcher comprises:

a delay receiving a local clock and passing a delayed clock; and

a NAND gate receiving said local clock and said delayed clock and providing stretched said clock pulses.

3. A CMOS write select circuit as in claim 2, wherein said NAND gate is a 2 input NAND gate and said delay is a group of series connected inverters.

4. A write select circuit as in claim 1, wherein said write select circuit is a CMOS write select circuit and said READ/WRITE decode is a dynamic decode comprising:

a pair of series connected complementary field effect transistors (FETs), stretched said clock pulses being connected to the gates of said pair, a common drain connection of said pair being a READ/WRITE decode output; and

at least one write enable FET, selectively providing a path to ground for said pair.

5. A CMOS write select circuit as in claim 4, wherein said write driver comprises:

a pseudo latch P-type FET (PFET), said READ/WRITE decode output being connected to a conductive terminal of said pseudo latch PFET; and

a first inverter, said READ/WRITE decode output being an input to said first inverter.

6. A CMOS write select circuit as in claim 5, said write driver further comprising a second inverter driving said write select pulses, an output of said first inverter being an input of said second inverter.

7. A bit decoder comprising:

a pulse stretcher stretching clock pulses;

a bit decode selectively passing stretched said clock pulses responsive to a column address; and

a column driver receiving passed said stretched clock pulses and driving said column select pulses responsive to received said stretched clock pulses.

8. A bit decoder as in claim 7, wherein said bit decoder is a CMOS bit decoder and said pulse stretcher comprises:

a delay receiving a local clock and passing a delayed clock; and

a NAND gate receiving said local clock and said delayed clock and providing stretched said clock pulses.

9. A CMOS bit decoder as in claim 8, wherein said NAND gate is a 2 input NAND gate and said delay is a group of series connected inverters.

10. A bit decoder as in claim 7, wherein said bit decoder is a CMOS bit decoder and said bit decode is a dynamic decode comprising:

an n bit address decode connected between a decode node and a common source node;

a restore FET connected between a supply and said decode node;

a complementary pair of enable FETs, a first of said complementary pair being connected between said supply and a decode out of said bit decode, a second of said complementary pair being connected between a supply return and said common source node, the gate of said restore FET and of each of said complementary pair being connected to an output of said pulse stretcher;

a decode out FET connected between said decode out and said enable node, said decode node being connected to the gate of said decode out FET; and

a first pseudo latch FET connected between said supply and said decode node and gated by said decode out.

11. A CMOS bit decoder as in claim 10, wherein said write driver comprises:

a second pseudo latch FET connected between said supply and said decode out; and

a decode out inverter driving said column select pulses and connected to the gate of said second pseudo latch FET, said decode out being an input to said decode out inverter.

12. A CMOS bit decoder as in claim 11, wherein each of said decode out FET and said second of said complementary pair are N-type FETs and each of said restore FET, said first of said complementary pair, said first pseudo latch FET and said second pseudo latch FET are P-type FETs.

13. A CMOS bit decoder as in claim 12, wherein said n-bit address decode comprises n parallel NFETs connected between said decode node and said common source node and said decode out inverter comprises a pair of parallel PFETs.

14. A random access memory (RAM) comprising:

a memory array comprising a plurality of memory cells organized as a plurality of rows and columns;

a word decoder selecting a word line identifying one of said rows responsive to a memory location access request;

a bit decoder providing column select pulses responsive to said memory location access request;

a column select selecting a column responsive to said column select pulses; and

a write select selectively providing write select pulses, said write select pulses being wider than corresponding said column select pulses.

15. A RAM as in claim 14, wherein said write select comprises:

a pulse stretcher stretching clock pulses;

a READ/WRITE decode selectively passing stretched said clock pulses responsive to a write select signal; and

a write driver receiving passed said stretched clock pulses and driving said write select pulses responsive to received said stretched clock pulses.

16. A RAM as in claim 15, wherein said RAM is a CMOS RAM and said READ/WRITE decode is a dynamic decode comprising:

a pair of series connected complementary field effect transistors (FETs), stretched said clock pulses being connected to the gates of said pair, a common drain connection of said pair being a READ/WRITE decode output; and

at least one write enable FET, selectively providing a path to ground for said pair.

17. A CMOS RAM as in claim 16, wherein said write driver comprises:

a pseudo latch P-type FET (PFET), said READ/WRITE decode output being connected to the drain of said pseudo latch PFET; and

a first inverter, said READ/WRITE decode output being an input to said first inverter.

18. A CMOS RAM as in claim 17, said write driver further comprising a second inverter driving said write select pulses, an output of said first inverter being an input of said second inverter.

19. A RAM as in claim 15, wherein said bit decoder comprises:

a pulse stretcher stretching clock pulses;

a bit decode selectively passing stretched said clock pulses responsive to a column address; and

a column driver receiving passed said stretched clock pulses from said bit decode and driving said column select pulses responsive to received said stretched clock pulses.

20. A RAM as in claim 19, wherein said RAM is a CMOS RAM and said bit decode is a dynamic decode comprising:

an n bit address decode connected between a decode node and a common source node;

a restore FET connected between a supply and said decode node;

a complementary pair of enable FETs, a first of said complementary pair being connected between said supply and a decode out of said bit decode, a second of said complementary pair being connected between a supply return and said common source node, the gate of said restore FET and of each of said complementary pair being connected to an output of said pulse stretcher;

a decode out FET connected between said decode out and said enable node, said decode node being connected to the gate of said decode out FET; and

a first pseudo latch FET connected between said supply and said decode node and gated by said decode out.

21. A CMOS RAM as in claim 20, wherein said write driver comprises:

a second pseudo latch FET connected between said supply and said decode out; and

a decode out inverter driving said column select pulses and connected to the gate of said second pseudo latch FET, said decode out being an input to said decode out inverter.

22. A CMOS RAM as in claim 21, wherein each of said decode out FET and said second of said complementary pair are N-type FETs and each of said restore FET, said first of said complementary pair, said first pseudo latch FET and said second pseudo latch FET are P-type FETs.

23. A CMOS RAM as in claim 22, wherein said n-bit address decode comprises n parallel NFETs connected between said decode node and said common source node and, said decode out inverter comprises a pair of parallel P FETs.

24. A RAM as in claim 19, wherein each said pulse stretcher comprises:

a delay receiving a local clock and passing a delayed clock; and

a NAND gate receiving said local clock and said delayed clock and providing stretched said clock pulses.

25. A RAM as in claim 24, wherein said delay in said write select is twice as long as said delay in said bit decoder.

26. A RAM as in claim 25, wherein each said NAND gate is a 2 input NAND gate and each said delay is a group of series connected inverters.

27. A RAM as in claim 25, wherein said column select pulses are wider than word line pulses provided to said selected word line by said word decoder.

28. A RAM as in claim 27, wherein said plurality of memory cells are static RAM (SRAM) cells.

29. A RAM as in claim 27, wherein said SRAM cells are 2 port SRAM cells.

30. A RAM as in claim 27, wherein said RAM is an SRAM macro on an integrated circuit (IC) chip.

31. A CMOS integrated circuit (IC) chip including a static random access memory (SRAM), said SRAM comprising:

an array comprising a plurality of SRAM cells organized as a plurality of rows and columns;

a word decoder selectively providing a word line pulse to a word line selected from one of said rows, said word line pulse being synchronized to a local clock, said word decoder pulsing the selected said word line responsive to an access request;

a bit decoder comprising:

a pulse stretcher stretching clock pulses,

a bit decode selectively passing stretched said clock pulses responsive to a column address, and

a column driver receiving passed said stretched clock pulses and driving a column select pulse responsive to each received one of said stretched clock pulses, said column select pulse being wider than a word line select pulse from said word decoder;

a column select selecting a column responsive to said column select pulse; and

a write select comprising:

a pulse stretcher stretching clock pulses,

a READ/WRITE decode selectively passing stretched said clock pulses responsive to a write select signal, and

a write driver receiving passed said stretched clock pulses from said READ/WRITE decode and driving a write select pulse responsive to each received one of said stretched clock pulses, each said write select pulse being wider than said column select pulse.

32. A CMOS IC as in claim 31, wherein each said pulse stretcher comprises:

a delay receiving said local clock and passing a delayed said local clock, said delay in said write select being longer than said delay in said bit decoder; and

a NAND gate receiving said local clock and providing said stretched clock pulses.

33. A CMOS IC as in claim 32, wherein each said NAND gate is a 2 input NAND gate and each said delay is a group of series connected inverters.

34. A CMOS IC as in claim 33, wherein said delay in said write select is twice as long as said delay in said bit decoder.

35. A CMOS IC as in claim 30, wherein said SRAM cells are 2 port SRAM cells.